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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/697,024 | NAM ET AL. | |
| | Examiner | Art Unit | |
| | Michael H. Caley | 2871 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/12/06 has been entered.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent Application Publication No. 2002/0071065) in view of Yoo et al. (U.S. Patent Application Publication No. 2001/0030718 "Yoo").**

Regarding claim 5, Lee discloses a manufacturing method of an array substrate for a liquid crystal display device, comprising:

forming a gate electrode (Figure 8D element 102) on a substrate (Figure 8D element 100) having a display region (Figure 7);

forming a gate insulating layer (Figure 8D element 106) on the gate electrode;

forming an active layer (Figure 8D element 108a) and an ohmic contact layer (Figure 8D element 108b) on the gate insulating layer over the gate electrode;

forming source (Figure 8D element 112) and drain (Figure 8D element 114) electrodes;

forming a pixel electrode (Figure 7 elements 116 and 117) contacting the drain electrode on the gate insulating layer;

forming an alignment layer (Figure 8D element 118) on the pixel electrode and the source and drain electrodes, wherein the alignment layer directly contacts the pixel electrode and the source and drain electrodes (Figure 8D); and

forming a data line (Figure 7 element 113) connected to the source electrode.

Lee fails to disclose the steps of forming a data pad at a non-display region and forming a data pad terminal contacting the data pad. Yoo, however, teaches forming a data pad (Figure 6D

element 120) and a data pad terminal contacting the data pad (Figure 6D element 124) in the non-display region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the display device disclosed by Lee to have a data pad at the non-display region and a data pad terminal contacting the data pad. One would have been motivated to provide a data pad and data pad terminal as proposed to provide a signal to the data line for controlling switching elements within the display region (Yoo: Page 2 [0018], Lee: Page 4 [0051]).

Regarding claims 6 and 7, Lee fails to disclose the data pad terminal and the pixel electrode as formed at the same time and as having the same material. Yoo, however, teaches the data pad terminal as formed at the same time and of the same material as the pixel electrode (Page 4 [0049]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the data pad terminal at the same time and of the same material as the pixel electrode. One would have been motivated to form the data pad terminal and the pixel electrode as proposed to benefit from a process using a reduced number of masks and manufacturing steps (Page 4 [0049], Page 2 [0021], Page 3 [0030]. As is known in the art, such a reduction in masking steps is beneficial to significantly reduce manufacturing costs and improve manufacturing yield (Page 2 [0020]).

Regarding claim 9, Lee fails to explicitly disclose at least one of the electrodes as formed by a dry etching method. Yoo, however, teaches a dry-etching process as advantageous for forming multiple display layers simultaneously (Page 4 [0048]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form at least one of the display electrodes from a dry-etching process. One would have been motivated to use the dry-etching process to reduce the number of steps in forming the TFT structures in the display device by forming multiple layers simultaneously and thus reduce manufacturing costs (Page 2 [0020]).

**Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yoo and in further view of Matsunaga et al. (U.S. Patent No. 5,510,918 "Matsunaga").**

Lee fails to disclose the pad terminal as extending to the display region. Matsunaga, however, teaches a pad terminal less susceptible to corrosion by extending the pad terminal to the display region beneath a passivation layer (Figures 8 and 19 element DTM; Column 12 lines 19-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the pad terminal disclosed by Lee to extend to the display region. One would have been motivated to extend the pad terminal to the display region to keep the resistance of the data terminal from increasing due to corrosion (Column 12 lines 26-30).

**Claims 10, 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yoo and in further view of Tanaka et al. (U.S. Patent Application Publication No. 2001/0035527 "Tanaka").**

Regarding claims 10 and 13, Lee fails to disclose one of the electrodes or ohmic contact layer as formed by a photolithography method using a photoresist. Tanaka, however, teaches a photolithography method using a photoresist to form at least one of the electrodes and the ohmic contact layer (Page 4 [0070], [0073], Page 5 [0075], [0080]) as part of a method of finely forming TFT and pixel electrode elements on a substrate (Page 1 [0004]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed at least one of the electrodes and the ohmic contact layer in the display device disclosed by Dohjo by a photolithography method using a photoresist. Tanaka teaches such a method as conventionally used to finely form display elements on the active matrix substrate (Page 1 [0004]). One would have been motivated to use such a technique to benefit from the ability to finely control the placement of the TFT elements at a high density according to conventional methods.

Regarding claims 11 and 14, Dohjo fails to disclose the photoresist used in the photolithography method as removed by a dry strip method (ashing). Tanaka, however, teaches such a photoresist removal method as beneficial to enable a reduction in the number of photolithography steps in forming the TFT electrodes and ohmic contact layer (Page 2 [0011]-[0013], Page 4 [0073], [0074], Page 6 [0086]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the photoresist by a dry strip method in the display device disclosed by Dohjo. One would have been motivated to apply such a method to reduce the number of photolithography steps (Page 2 [0011]-[0013]) and to configure the lateral dimensions of the layers such that impurities in the liquid crystal layer are prevented from entering the a-Si film (Page 6 [0086]).

**Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yoo and Tanaka and in further view of Okutani (U.S. Patent No. 5,135,608 "Okutani").**

Lee as modified by Tanaka discloses the dry strip method as using dry gases, but fails to disclose the use of $O_2$ as a base gas and $SF_6$ or $CF_4$ as a reactive gas. Okutani, however, teaches a mixture of $CF_4$ and $O_2$ as an alternative dry gas to $O_2$ alone in a dry strip method (Column 5 lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used $O_2$ as a base gas and $SF_6$ or $CF_4$ as a reactive gas in the dry strip method. One would have been motivated to use such a dry gas mixture as an engineering expediency to achieve the expected results of such a mixture such as a particular photoresist removal rate.

**Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yoo and Tanaka and in further view of Nakamura et al. (U.S. Patent No. 6,621,537 "Nakamura").**

Lee as modified by Tanaka fails to disclose the upper surface of the ohmic contact layer as etched to a depth between about 100 and about 700 Angstroms. Nakamura, however, teaches an etched ohmic contact film with a controllable thickness between 200 and 700 Angstroms (Column 8 lines 35-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the ohmic contact layer to have an etched thickness between 100 and 700 Angstroms and a thickness before etching of 400 and 1000 Angstroms. One would have been motivated to set the thickness before etching and the etched thickness as proposed to allow for controllability of the ohmic contact layer thickness according to a desired ON current for the TFT device (Column 8 lines 35-38).

**Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yoo and in further view of Choi (U.S. Patent No. 6,169,592).**

Lee fails to disclose the alignment layer as formed by a printing method. Choi, however, teaches the alignment layer as formed by a printing method (Column 2 line 10 – Column 3 line 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have constructed the alignment layer disclosed by Lee by means of a printing method. One would have been motivated to form the alignment layer by a printing method as taught by Choi to avoid the labor intensive processes of alternative alignment layer forming methods (Column 2 lines 13-15) while forming a display having satisfactory display characteristics (Column 2 lines 36-49).

**Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Lyu et al. (U.S. Patent No. 6,001,539 "Lyu").**

Tanaka discloses a method of manufacturing an array substrate for a liquid crystal display device comprising:

forming a thin film transistor (Figure 3 element 200) having a gate electrode (Figure 5A element 201), source (Figure 11 element 213) and drain (Figure 11 element 214) electrodes, an active layer (Figure 10 element 104), and an ohmic contact layer (Figure 11 element 109);

forming a pixel electrode (Figures 10 and 11 element 209) contacting the drain electrode;

wherein the ohmic contact layer is etched by a dry etching process (Page 5 [0075]);

wherein the formation of at least one of the electrodes, the active layer, and the ohmic contact layer are processed by a photolithography method using photoresists; and wherein a photoresist used in the formation of the ohmic contact layer is removed by a dry strip method using dry gases (Page 4 [0070], [0074]).

Tanaka fails to disclose the ohmic contact layer as etched and the photoresist used in forming the layer as removed in a same chamber. Lyu, however, teaches dry etching processes and dry strip processes as performable in a same dry-etching chamber to reduce the number of manufacturing steps (Column 5 lines 45-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the manufacturing method disclosed by Tanaka to include the step of dry etching the ohmic contact layer and removing the photoresist used in forming the layer in a same chamber. One would have been motivated to perform the two processes in the same chamber to reduce the number of manufacturing steps involved in forming the ohmic contact layer and reduce manufacturing costs.

**Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Lyu and in further view of Okutani.**

Tanaka as modified by Lyu discloses the dry strip method as using dry gases, but fails to disclose the use of $O_2$ as a base gas and $SF_6$ or $CF_4$ as a reactive gas. Okutani, however, teaches a mixture of $CF_4$ and $O_2$ as an alternative dry gas to $O_2$ alone in a dry strip method (Column 5 lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used $O_2$ as a base gas and $SF_6$ or $CF_4$ as a reactive gas in the dry strip method. One would have been motivated to use such a dry gas mixture as an engineering expediency to achieve the expected results of such a mixture such as a particular photoresist removal rate.

**Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Lyu and in further view of Nakamura.**

Tanaka discloses the ohmic contact layer as formed after the above dry strip method but fails to disclose the upper surface of the ohmic contact layer as etched to a depth between about

100 and about 700 Angstroms and a thickness before etching of 400 and 1000 Angstroms. Nakamura, however, teaches an etched ohmic contact film with a controllable thickness between 200 and 700 Angstroms (Column 8 lines 35-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the ohmic contact layer to have an etched thickness between 100 and 700 Angstroms and a thickness before etching of 400 and 1000 Angstroms. One would have been motivated to set the thickness before etching and the etched thickness as proposed to allow for controllability of the ohmic contact layer thickness according to a desired ON current for the TFT device (Column 8 lines 35-38).

### *Response to Arguments*

Applicant's arguments with respect to claims 5-22 have been considered but are moot in view of the new ground(s) of rejection.

### *Contact Information*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael H. Caley whose telephone number is (571) 272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael H. Caley
August 15, 2006